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| GLAST LAT SUBSYSTEM SPECIFICATION | Document # **LAT-SS-00352-01-D6** | Date Effective Draft 11/12/02 |
| | Responsible Engineer(s) Jonathan Ormes | Supersedes None |
| | Subsystem/Office ACD Subsystem | |
| Document Title **LAT ACD Subsystem Spec - Level IV Electronics Requirements** | | |

# Gamma-ray Large Area Space Telescope

# (GLAST)

# Large Area Telescope (LAT)

# Anticoincidence Detector (ACD)

# Subsystem Specification

# CHANGE HISTORY LOG

| Revision | Effective Date | Description of Changes | DCN # |
|---|---|---|---|
| 1 | | Initial Release | |
| | | | |
| | | | |
| | | | |
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# ACD Approvals

| | |
|---|---|
| Jonathan Ormes | Date |
| ACD Subsystem Manager | |
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# CONTENTS

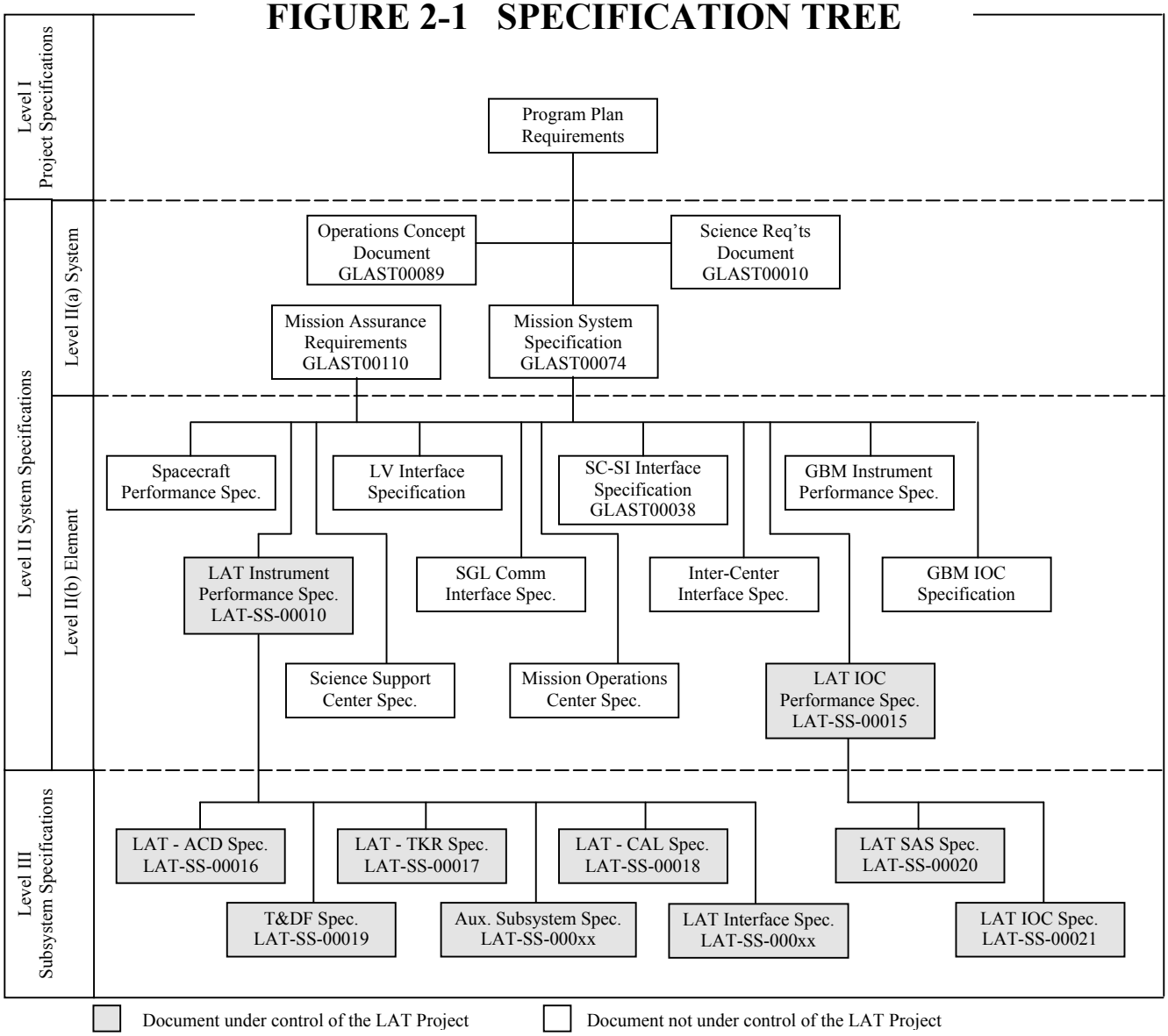
# 1 PURPOSE

This document defines level IV subsystem electronics requirements for the GLAST Large Area Telescope (LAT) Anticoincidence Detector (ACD).

# 2 SCOPE

This specification captures the GLAST LAT requirements for the ACD. This encompasses the subsystem level requirements and the design requirements for the ACD. The verification methods of each requirement are identified.

## FIGURE 2-1 SPECIFICATION TREE




This specification is identified in the specification tree of Figure 2-1.

# 3 DEFINITIONS

## 3.1 Acronyms

ACD - Anticoincidence Detector

FOV – Field of View

GLAST – Gamma-ray Large Area Space Telescope

IOC – Instrument Operations Center

IRD – Interface Requirements Document

LAT – Large Area Telescope

MIP – Minimum Ionizing Particle (see definition below)

MSS – Mission System Specification

PI – Principal Investigator

SAS – Science Analysis Software

SI/SC IRD – Science Instrument – Spacecraft Interface Requirements Document

SRD – Science Requirements Document

SSC – Science Support Center

TEM - Tower Electronics Module

TBD - To Be Determined

TBR – To Be Resolved

## 3.2 Definitions

□sec, □s – Microsecond, $10^{-6}$ second

Analysis – A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.

Background Rejection – The ability of the instrument to distinguish gamma rays from charged particles.

Backsplash – Secondary particles and photons originating from very high-energy gamma-ray showers in the calorimeter giving unwanted ACD signals.

cm – centimeter

Cosmic Ray - Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations.

Demonstration – To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.

eV – Electron Volt

Field of View – Integral of effective area over solid angle divided by peak effective area.

GeV – Giga Electron Volts. $10^9$ eV

Inspection – To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.

MeV – Million Electron Volts, $10^6$ eV

Minimum Ionizing Particle (MIP) – The mean signal from cosmic ray produced air shower muons at sea level normally incident on a scintillator tile. It corresponds to approximately 1.9 MeV per cm of scintillator.

nsec, ns – Nanosecond, $10^{-9}$ second

ph – photons

s, sec – seconds

Simulation – To examine through model analysis or modeling techniques to verify conformance to specified requirements

Testing – A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.

Validation – Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.

Verification – Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

VETO - The signal from an individual ACD scintillator tile that indicates an energy deposit of at least ~0.3 MIP (~500 keV) in an ACD scintillator tile, or about 20% of that amount in one of the scintillating fiber ribbons. This threshold is set to be exceeded for a very high fraction of MIPs in the presence of all fluctuations in their energy deposit in the scintillator tiles. The VETO signals from individual tiles and ribbons are combined with information from the tracker and calorimeter to decide whether or not to reject events as background.

# 4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the ACD concept and its requirements include the following:

LAT-SS-00016, LAT ACD Subsystem Specification - Level III Requirements, June, 2001

LAT-GE-00009, "LAT Science Requirements Document–Level II Specification", August 6, 2000.

LAT-SS-00010, "GLAST LAT Performance Specification", August 2000

LAT-SS-00047, "LAT Mechanical Performance Specification"

GSFC 433-MAR-0001, "Mission Assurance Requirements (MAR) for Gamma-Ray Large Area Telescope (GLAST) Large Area Telescope (LAT)", June 9, 2000.

"GLAST Large Area Telescope Flight Investigation: An Astro-Particle Physics Partnership Exploring the High-Energy Universe", proposal to NASA, P. Michelson, PI, November, 1999.

# 5 REQUIREMENTS

## 5.1 System Description

The LAT science instrument consists of an Anticoincidence Device (ACD), a silicon-strip detector tracker (TKR), a hodoscopic CsI calorimeter (CAL), and a Trigger and Dataflow system (T&DF). The principal purpose of the LAT is to measure the incidence direction, energy and time of cosmic gamma rays. The measurements are streamed to the spacecraft for data storage and subsequent transmittal to ground-based analysis centers. Signals produced by the ACD are used by the T&DF system to identify cosmic ray electrons and nuclei entering the instrument.

The ACD detects energetic cosmic ray electrons and nuclei for the purpose of removing these backgrounds. It is the principle source for detection of incident particles other than gamma rays. This detector array covers the top and 4 sides of the TKR. It consists of an array of 89 plastic scintillator tiles (25 on the LAT top, 16 on each of the 4 sides, all 1 cm thick, various sizes), plus 8 scintillating fiber "ribbons" that cover the gaps between the tiles. Each scintillator tile is read by 2 PMT's (baseline: Hamamatsu R4443; designated "A" and "B") via waveshifting fibers (and in some cases, clear optical fiber extensions).

The PMT's and the ACD electronics will be located around the base of the ACD, in the Base Electronics Assembly (BEA). The 25 waveshifting fiber bundles and clear fiber extensions from the ACD Top will be routed down 2 opposite sides of the ACD (12 and 13), so that those two sides of the BEA will be more heavily populated than the remaining two sides. Each assembly of one tile plus the two associated waveshifting fiber bundles and clear fiber extensions denoted as a Tile Detector Assembly (TDA).

On each of the two opposite LAT sides (±Y) that contain TKR radiators, the BEA will house two ACD electronics boards, one for "A" PMT's and one for "B" PMT's. On each of the remaining two LAT sides (non-radiator), the BEA will house four ACD electronics boards, two associated with "A" PMT's and two associated with "B" PMT's. Each ACD electronics board will be capable of servicing 18 PMT's, although they will vary with regard to numbers of unused electronics channels. All 12 of the ACD electronics boards are nominally identical.

Each ACD electronics board will contain a high voltage bias supply (HVBS), which is capable of providing the necessary high voltage for all 18 associated PMT's. All 18 PMT's associated with a specific board will receive the same high voltage level.

Each ACD electronics board will contain 18 channels of analog, analog-to-digital, and digital processing electronics, as well as command reception and distribution logic and data collection and transmission logic.

Each ACD electronics board interfaces to the LAT via the ACD Tower Electronics Module (TEM). The TEM receives all signals and data from the ACD and sends commands to the ACD. All digital communications between the ACD and the TEM will be via standard LVDS protocol.

Science signals from the TDA's and their associated PMT's are defined in terms of MIP's,

the signal generated by a minimum-ionizing singly-charged particle traversing a tile in a direction normal to its surface. To provide a meaningful electronics specification, the definition of a MIP must be normalized to the electrical charge delivered by each of the two PMT's in response to a MIP. The following parameters are assumed for the MIP calculation:

10 photoelectrons per PMT per MIP

PMT gain of 400,000

The result is that **1 MIP** produces a PMT anode signal of **0.64 pC**.

In the requirements shown below, allowance has been made (and noted) for differential degradation of the PMT's within a board. This effect forces a broadening of the range of adjustability of the discriminators in sections 5.3, 5.6, and 5.9.2.

## 5.2 Charged Particle Detection

The ACD shall produce both fast and slow VETO signals in response to PMT signals resulting from charged particles traversing the ACD tiles and ribbons.

## 5.3 Adjustable Threshold on VETO Detection of Charged Particles

The threshold for VETO detection of charged particles shall be adjustable from 0.064 to 1.28 pC (0.10 to 2.0 MIP), with a step size of ≤0.032 pC (0.05 MIP). This range has been broadened to compensate for PMT differential degradation.

## 5.4 False VETO due to Electrical Noise

The total ACD false VETO trigger rate due to noise shall be less than 10 kHz at 0.096 pC (0.15 MIP) threshold (assuming 1 μs VETO pulses).

## 5.5 High-Threshold Detection

The ACD shall detect pulses due to highly-ionizing particles, carbon-nitrogen-oxygen or heavier nuclei, denoted High-Level Threshold or High-Level Discriminator (HLD), which produce signals from 20 pC to 640 pC. Each ACD electronics board shall OR up to 18 HLD outputs to generate a single HLD_OR signal for transmission to the ACD TEM.

## 5.6 Adjustable High-Threshold

The High-Level Threshold shall be adjustable for PMT signals from 12.8 to 40.96 pC (20 to 64 MIP) in steps of ≤0.64 pC (1 MIP). This range has been broadened to compensate for PMT differential degradation.

## 5.7 Level 1 Trigger Acknowledge

The ACD electronics shall accept from the ACD TEM a Level 1 Trigger Acknowledge signal (TACK; see GLAST LAT - CONCEPTUAL DESIGN OF THE ELECTRONICS, TRIGGER & DATAFLOW SYSTEM, LAT-SS-287.0) and respond by digitizing and latching data, as described below, for transmission to the TEM.

## 5.8 Signals

### 5.8.1 Fast VETO Signal Latency

The fast VETO signal latency shall be 50 $\leq t_{latent} \leq$ 600 ns from the time of particle passage. The time jitter in the VETO pulses during this latency window shall be ±200 ns relative to particle passage.

### 5.8.2 Fast VETO Signal Width

The Fast VETO output signal shall have a minimum width of 300 ns.

For a nominal 0.64 pC (1 MIP) signal, the Fast VETO output signal shall have a width of ±1.2 μs

For a signal of 640 pC (equivalent to 1000 MIP's), the fast VETO signal shall be ±10 μs.

The Fast VETO output signal shall be longer than the time for analog baseline recovery to within 0.05 MIP of the original baseline, to prevent change of threshold for following VETO's. (Assuming a signal amplitude of 2 Volts for a full-scale signal of 10 MIP, 0.05 MIP is equivalent to 0.010 V.)

### 5.8.3 Fast VETO Retriggering

The Fast VETO discriminator shall be capable of retriggering less than 50 ns after the trailing edge of the VETO output signal.

### 5.8.4 Logic VETO Signal

A map of VETO signals shall be generated for each TACK, indicating which ACD PMT's produced signals above their thresholds within 200 ns of the time of the event causing the TACK.

### 5.8.5 Logic VETO Signal Latency

In response to a TACK, the map of VETO signals shall be latched by the time the ADC conversions are complete.

### 5.8.6 High-Threshold Signal Latency

A highly-ionizing particle hitting the top or upper side row of tiles of the ACD shall produce a High-Threshold fast signal that will be delivered to the hardware trigger logic with

latency of no more than that defined for the fast VETO in specification 5.8.1. Command-selected signals out of the eighteen (18) High-Threshold (HLD) fast signals generated on a single electronics board shall be OR'ed to produce a single signal for transmission to the ACD TEM.

### 5.8.7 Discriminator Masking

Each ACD electronics board shall have the capability to disable any combination of the Fast VETO and HLD discriminator outputs.

### 5.8.8 ACD Trigger Primitives

The ACD will produce no trigger primitives internally. The VETO signals caused by the individual PMT's will be transmitted to the ACD TEM, where they will be OR'ed together (for each tile or ribbon), and used by the the TEM to generate trigger primitives.

## 5.9 Performance Monitoring and Calibration

The ACD TEM will scale and telemeter count rates for ACD VETO and HLD signals, as well as various trigger primitives. An ACD low-threshold signal will allow zero suppression of the pulse height data transmission to the data acquisition system. ACD voltages and currents will be monitored by the ACD-TEM.

### 5.9.1 Low-Threshold Signal

The ACD shall detect energy deposits above an adjustable threshold nominally at 0.064 pC (0.1 MIP) and produce Low-Threshold signals.

### 5.9.2 Low-Threshold Adjustability

The Low-Threshold shall be adjustable from 0.032 pC to 0.64 pC (0.05 to 1.0 MIP), with a step size of □0.032 pC (0.05 MIP). This range has been broadened to compensate for PMT differential degradation.

### 5.9.3 Signal Content

When a TACK signal is received (approx. ~2.5 □s after particle passage), the ACD electronics shall digitize all PMT signal amplitudes with the following precision:

- for a pulse below 6.4 pC (10 MIP), precision of <0.0128 pC (0.02 MIP) or 5%, whichever is larger;
- for a pulse above 6.4 pC (10 MIP), precision of □0.64 pC (1 MIP) or 2%, whichever is larger.
- The maximum signal amplitude to be digitized is 640 pC (1000 MIP).

### 5.9.4 Pulse Height Measurement Latency

The PMT pulse amplitudes shall be digitized, and the resulting data transmitted to the ACD-TEM, within 22 μs after receipt of TACK.

### 5.9.5 Integral Non-Linearity

The analog signal processing chain shall exhibit integral non-linearity of ±2% over the top 95% of the signal input range.

### 5.9.6 Differential Non-Linearity

The analog signal processing chain shall exhibit differential non-linearity of no more that ±_LSB, or 1/2048 of full scale, whichever is greater, over the middle 95% of the signal input range.

### 5.9.7 Temperature Stability

The analog signal processing chain shall exhibit temperature stability of gain better than 500 ppm per degree C over the range -20C to +45C

For both the low range (0 to 6.4 pC, = 10 MIPs) and the high range (6.4 to 640 pC, 10 to 1000 MIPS), the analog signal processing chain shall exhibit temperature stability of its baseline better than 0.05% of full scale per degree C.

### 5.9.8 Test Pulse Injection

For test purposes, the ACD electronics shall incorporate the capability to be artificially stimulated via commands (maximum test level ~40 pC).

### 5.9.9 Digital Housekeeping

The state of all ACD command registers shall be available for readout via TEM commands.

The ACD TEM will scale all ACD VETO and HLD rates and transmit the results in low rate telemetry.

### 5.9.10 Temperature Monitoring

For each ACD electronics board, an analog temperature transducer signal shall be transmitted to the ACD TEM for digitization and low-rate telemetry.

## 5.10 High Voltage Bias Supply Requirements

### 5.10.1 HVBS Output Voltage Range

Each HVBS shall be able to operate between +400 V and +1375 V.

### 5.10.2 HVBS Output Current

At maximum output voltage, each HVBS shall be capable of supplying a total output current of 60 μA. The nominal output current will be 36 μA.

### 5.10.3 HVBS Limiting Output Current

The limiting output current of each HVBS shall be ~80 μA.

### 5.10.4 HVBS Output Voltage Adjustment

The HVBS output voltage shall be programmable via an analog input voltage, 0.00 to 2.50 V.

### 5.10.5 HVBS Input Power

Each HVBS shall operate from a supply voltage of 28±6 V, with possible input ripple of 10 mV (frequency range 50 Hz to 50 MHz).

### 5.10.6 HVBS Line and Load Regulation

The HVBS output voltage shall be regulated to ±0.5% for all combinations of input voltage and load current.

### 5.10.7 HVBS Output Ripple

The HVBS output voltage ripple shall not exceed ±2 mV p-p over the frequency range 100 Hz to 50 MHz.

### 5.10.8 HVBS Power Dissipation

The HVBS power dissipation at maximum output voltage and limiting current shall be ≤300 mW.

### 5.10.9 HVBS Ramp Up/Down Time

For either application or removal of input power, the time for the HVBS output voltage to reach its final level (for turn-on, within regulation tolerance) shall be between 5 and 30 seconds.

### 5.10.10 HVBS Temperature Stability

The HVBS temperature stability shall be no worse than 500 ppm/C.

### 5.10.11 HVBS Output Voltage Monitoring

The HVBS shall provide a linear output voltage monitor (for transmission to the ACD TEM) in the range 0.0 to 2.5 V.

#### 5.10.12 HVBS Ground Isolation

The DC impedance between input and output grounds shall be 100 ohms ±20%.

#### 5.10.13 HVBS Oscillator Frequency

The HVBS shall utilize an oscillator frequency ≥100 kHz.

#### 5.10.14 HVBS EMI and Susceptibility

The HVBS shall neither generate nor be susceptible to electromagnetic interference exceeding the GLAST LAT EMI/EMC test requirement, TBD.

### 5.11 PMT Bias Chain Requirements

#### 5.11.1 PMT Bias Chain Total Resistance

The total resistance of a PMT bias chain shall be such as to result in a nominal current of 2 μA at the maximum HVBS voltage.

#### 5.11.2 PMT Bias Chain Filter Resistance

Ten percent (nominal) of the total resistance of the bias chain shall be in a filter resistor(s) at the high voltage input.

#### 5.11.3 PMT Bias Chain Resistor Distribution

The number and values of the remaining resistors in the bias chain shall be TBD (depending upon the choice of PMT).

#### 5.11.4 PMT Anode Signal Coupling

The PMT anode signal shall be coupled into the associated analog electronics via two capacitors of 680 pF (TBD) in series. A charge leakage bleed-off resistor of ~10 megohm shall be incorporated on the low-voltage side of the capacitor pair.

#### 5.11.5 PMT Bias Chain Load Resistor

A load resistor of ~10 kilohms shall be incorporated into the bias network.

#### 5.11.6 PMT Bias Chain Dynode Decoupling

The resistors biasing the last three dynode stages shall be bypassed by capacitors to prevent excessive loading by very large pulses.

## 5.12 Radiation Tolerance

The ACD electronics shall remain within specifications after a total ionizing radiation dose of 10 kRad/Si.

## 5.13 Reliability

### 5.13.1 ACD Electronics Reliability

No single failure in the ACD electronics shall result in complete loss of signal from more than one detector element (tile or ribbon). The overall calculated reliability of an ACD event processor electronics board shall be at least 0.98 per year.

### 5.13.2 ACD System Reliability

The probability of the loss of both VETO signals from a specific scintillator tile shall be less than 1%/year (TBR). The probability of the loss of VETO signals from a scintillator ribbon shall be less than 5%/year (TBR).

### 5.13.3 Latchup Tolerance

The ACD electronics shall not be susceptible to latchup, or if susceptible, will autonomously detect a latchup and recycle power on the affected part.

### 5.13.4 Single Event Upset Tolerance

A single event upset (SEU) shall not cause the ACD electronics to transition to an unsafe state.

## 5.14 Commands

### 5.14.1 Detector On/Off Commands

The ACD-TEM will implement commands to allow each group of 18 PMT's to be powered on and off together.

### 5.14.2 Detector Gain Commands

The ACD shall implement adjustability of the high voltage applied to the group of 18 PMT's associated with a single board.

### 5.14.3 Electronics On/Off Commands

The ACD-TEM will implement commands to allow each ACD electronics board to be separately powered on and off.

#### 5.14.4 VETO Threshold Commands

The ACD shall implement adjustability of the VETO threshold for each PMT.

#### 5.14.5 High-Threshold Commands

The ACD shall implement adjustability of the High-Threshold for each PMT.

#### 5.14.6 ACD Monitoring Commands

The ACD shall implement adjustability of the monitoring functions of the ACD electronics, including the Low-Threshold for each PMT.

#### 5.14.7 Trigger Acknowledge (TACK) Format

As defined in LAT-ACD Interface Control Document

#### 5.14.8 Command Format

As defined in LAT-ACD Interface Control Document

### 5.15 Output Data Formats

As defined in LAT-ACD Interface Control Document

### 5.16 Power Consumption

The ACD total electronics power consumption shall not exceed 37 W.

### 5.17 Total Electronics Mass

As defined in LAT-ACD Interface Control Document

### 5.18 Environmental Requirements

The ACD electronics shall meet the structural and thermal environment requirements defined in the LAT-ACD Subsystem Mechanical Interface Control Document, LAT-DS-00241.

### 5.19 Performance Life

The ACD shall maintain the specified performance for a minimum of five years in orbit.

### 5.20 Operation in High Rate Conditions

The ACD photomultiplier bias supplies shall switch into a low-gain mode via ACD-TEM command to protect the phototubes in very high intensity particle conditions (> 10 kHz in an individual tile) such as the South Atlantic Anomaly.

### 5.20.1 Notification of Mode Change

The ACD shall identify times when it switches into low-gain mode for high counting rate conditions.

### 5.20.2 Tile Linear Response

Each ACD PMT and its associated electronics shall be capable of operating within the specifications above at MIP rates up to 3 kHz.

## 5.21 Testability

The ACD electronics shall incorporate additional capabilities as needed to enable thorough and efficient testing, throughout the GLAST mission, of the functions required of the ACD. The single exception to this requirement is that the test pulsers on the ACD electronics board shall have a maximum output of ~40 pC (~60 MIPs). For board-level testing, a test fixture shall be provided that will allow testing over the full 640 pC (1000 MIP) range of the high-range PHA's. In flight, testing and calibration over the full range will be possible by utilizing cosmic ray nuclei through iron (Fe). At subsystem- and LAT-level, testing of the high range PHA's will be possible only up to the ~40 pC (~60 MIP) maximum of the test pulsers.

# 6 VERIFICATION STRATEGY

The verification strategy will test, analyze (may include modeling/simulation), inspect, or demonstrate all requirements of section 5 to ensure that the instrument meets the requirements of this specification. The matrix below indicates the methods of verification employed to verify the science performance.

**Table 6-1. Requirements Verification Matrix**

Note: Verification methods are T = Test, A = Analysis, D = Demonstrate, I = Inspect

| Req | Title | Summary | Verif |
|---|---|---|---|
| 5.2 | Charged Particle Detection | The ACD shall produce both fast and slow VETO signals in response to PMT signals resulting from charged particles traversing the ACD tiles and ribbons. | T |
| 5.3 | Adjustable Threshold on VETO Detection of Charged Particles | The threshold for detecting charged particles shall be adjustable from 0.064 to 1.28 pC, with a step size of □0.032 pC. | T |
| 5.4 | False VETO due to Electrical Noise | The total ACD false VETO trigger rate due to noise shall be less than 10 kHz at 0.096 pC (0.15 MIP) threshold (assuming 1 □s VETO pulses). | A,T |
| 5.5 | High-Threshold Detection | The ACD shall detect pulses due to highly-ionizing particles, carbon-nitrogen-oxygen or heavier nuclei, denoted High-Level Threshold or High-Level Discriminator (HLD), which produce signals from 20 pC to 640 pC. Each ACD electronics board shall OR up to 18 HLD outputs to generate a single HLD_OR signal for transmission to the ACD TEM. | A,T |
| 5.6 | Adjustable High-Threshold | The High-Level Threshold shall be adjustable for PMT signals from 12.8 to 40.96 pC (20 to 64 MIP) in steps of □0.64 pC (1 MIP). | A,T |
| 5.7 | Level 1 Trigger Acknowledge | The ACD electronics shall accept from the ACD TEM a Level 1 Trigger Acknowledge signal and respond by digitizing and latching data. | A,T |
| 5.8.1 | Fast VETO Signal Latency | The fast VETO signal latency shall be 50□$t_{latent}$□600 ns from the time of particle passage. The time jitter in the VETO pulses shall be □200 ns relative to particle passage. | A,T |
| 5.8.2 | Fast VETO Signal Width | The Fast VETO output signal shall have a minimum width of 300 ns. For a nominal 0.64 pC (1 MIP) signal, the Fast VETO output signal shall have a width of □1.2 □s. For a signal of 640 pC (equivalent to 1000 MIP's), the fast VETO signal shall be □10 □s. The Fast VETO output signal shall be longer than the time for analog baseline recovery to within 0.05 MIP of the original baseline, to prevent change of threshold for following VETO's. (Assuming a signal amplitude of 2 Volts for a full-scale signal of 10 MIP, 0.05 MIP is equivalent to 0.010 V.) | A,T |
| 5.8.3 | Fast VETO Retriggering | The Fast VETO discriminator shall be capable of retriggering less than 50 ns after the trailing edge of the VETO output signal. | A,T |
| 5.8.4 | Logic VETO Signal | A map of VETO signals shall be generated for each TACK, indicating which ACD PMT's produced signals above their thresholds within 200 ns of the time of the event causing the TACK. | A,T |
| 5.8.5 | Logic VETO Signal Latency | In response to a TACK, the map of VETO signals shall be latched by the time the ADC conversions are complete | A,T |

| Req | Title | Summary | Verif |
|---|---|---|---|
| | | | |
| 5.8.6 | High-Threshold Signal Latency | A highly-ionizing particle hitting the top or upper side row of tiles of the ACD shall produce a High-Threshold fast signal that will be delivered to the hardware trigger logic with latency of no more than that the latency as defined for the fast VETO in specification 5.8.1. Command-selected signals out of the eighteen (18) High-Threshold fast signals generated on a single electronics board shall be OR'ed to produce a single signal for transmission to the ACD TEM. | A,T |
| 5.8.7 | Discriminator Masking | Each ACD electronics board shall have the capability to disable any combination of the Fast VETO and HLD discriminator outputs. | A,D |
| 5.8.8 | ACD Trigger Primitives | The ACD will produce no trigger primitives internally. The VETO signals caused by the individual PMT's will be transmitted to the ACD TEM, where they will be OR'ed together (for each tile or ribbon), and used by the the TEM to generate trigger primitives. | D |
| 5.9 | ACD Performance Monitoring | The ACD TEM will scale and telemeter count rates for ACD VETO and HLD signals, as well as various trigger primitives. An ACD low-threshold signal will allow zero suppression of the pulse height data transmission to the data acquisition system. ACD voltages and currents will be monitored by the ACD TEM. | D |
| 5.9.1 | Low-Threshold Signal | The ACD shall detect energy deposits above an adjustable threshold nominally at 0.064 pC and produce Low-Threshold signals. | A,T |
| 5.9.2 | Low-Threshold Adjustability | The Low-Threshold shall be adjustable from 0.032 pC to 0.64 pC, with a step size of □0.032 pC. | A,T |
| 5.9.3 | Signal Content | When a TACK signal is received, the ACD electronics shall digitize all PMT signal amplitudes with the following precision:<br>- for a pulse below 6.4 pC, precision of <0.0128 pC or 5%, whichever is larger;<br>- for a pulse above 6.4 pC, precision of □0.64 pC (1 MIP) or 2%, whichever is larger.<br>- The maximum signal amplitude to be digitized is 640 pC (1000 MIP). | A,T |
| | | | |
| 5.9.4 | Pulse Height Measurement Latency | The PMT pulse amplitudes shall be digitized, and the resulting data transmitted to the ACD-TEM, within 22 □s after receipt of TACK. | A,T |
| 5.9.5 | Integral Non-Linearity | The analog signal processing chain shall exhibit integral non-linearity of □2% over the top 95% of the signal input range. | A,T |
| 5.9.6 | Differential Non-Linearity | The analog signal processing chain shall exhibit differential non-linearity of no more that ±_LSB, or 1/2048 of full scale, whichever is greater, over the middle 95% of the signal input range. | A,T |
| 5.9.7 | Temperature Stability | The analog signal processing chain shall exhibit temperature stability of gain better than 500 ppm per degree C over the range -20C to +45C. For both the low range (0 to 6.4 pC, = 10 MIPs) and the high range (6.4 to 640 pC, 10 to 1000 MIPS), the analog signal processing chain shall exhibit temperature stability of its baseline better than 0.05% of full scale per degree C. | A,T |
| 5.9.8 | Test Pulse Injection | For test purposes, the ACD electronics shall incorporate the capability to be artificially stimulated via commands (maximum test level ~40 pC). | A,D |

| Req | Title | Summary | Verif |
|---|---|---|---|
| 5.9.9 | Digital Housekeeping | The state of all ACD command registers shall be available for readout via TEM commands.<br>The ACD TEM will scale all ACD VETO and HLD rates and transmit the results in low rate telemetry. | D |
| 5.9.10 | Temperature Monitoring | For each ACD electronics board, an analog temperature transducer signal shall be transmitted to the ACD TEM for digitization and low-rate telemetry. | D |
| 5.10.1 | HVBS Output Voltage Range | Each HVBS shall be able to operate between +400 V and +1375 V. | A,D |
| 5.10.2 | HVBS Output Current | At maximum output voltage, each HVBS shall be capable of supplying a total output current of 60 μA. The nominal output current will be 36 μA. | A,D |
| 5.10.3 | HVBS Limiting Output Current | The limiting output current of each HVBS shall be ~80 μA. | A,T |
| 5.10.4 | HVBS Output Voltage Adjustment | The HVBS output voltage shall be programmable via an analog input voltage, 0.00 to 2.50 V. | A,D |
| 5.10.5 | HVBS Input Power | Each HVBS shall operate from a supply voltage of 28±6 V, with possible input ripple of 10 mV (frequency range 50 Hz to 50 MHz). | A,D |
| 5.10.6 | HVBS Line and Load Regulation | The HVBS output voltage shall be regulated to ±0.5% for all combinations of input voltage and load current. | A,T |
| 5.10.7 | HVBS Output Ripple | The HVBS output voltage ripple shall not exceed ±2 mV p-p over the frequency range 100 Hz to 50 MHz. | A,T |
| 5.10.8 | HVBS Power Dissipation | The HVBS power dissipation at maximum output voltage and limiting current shall be <300 mW. | A,D |
| 5.10.9 | HVBS Ramp Up/Down Time | For either application or removal of input power, the time for the HVBS output voltage to reach its final level (for turn-on, within regulation tolerance) shall be between 5 and 30 seconds. | A,D |
| 5.10.10 | HVBS Temperature Stability | The HVBS temperature stability shall be no worse than 500 ppm/C. | A,T |
| 5.10.11 | HVBS Output Voltage Monitoring | The HVBS shall provide a linear output voltage monitor (for transmission to the ACD TEM) in the range 0.0 to 2.5 V. | A,D |
| 5.10.12 | HVBS Ground Isolation | The DC impedance between input and output grounds shall be 100 ohms ±20%. | A,D |
| 5.10.13 | HVBS Oscillator Frequency | The HVBS shall utilize an oscillator frequency ≥100 kHz. | A,D |
| 5.10.14 | HVBS EMI and Susceptibility | The HVBS shall neither generate nor be susceptible to electromagnetic interference exceeding the GLAST LAT EMI/EMC test requirement, 433-RQMT-0005. | A,T |
| 5.11.1 | PMT Bias Chain Total Resistance | The total resistance of a PMT bias chain shall be such as to result in a nominal current of 2 μA at the maximum HVBS voltage. | A,D |
| 5.11.2 | PMT Bias Chain Filter Resistance | Ten percent (nominal) of the total resistance of the bias chain shall be in a filter resistor(s) at the high voltage input. | A,D |
| 5.11.3 | PMT Bias Chain Resistor Distribution | The number and values of the remaining resistors in the bias chain shall be TBD (depending upon the choice of PMT). | A,D |
| | 4 | | |
| 5.11.4 | PMT Anode Signal Coupling | The PMT anode signal shall be coupled into the associated analog electronics via two capacitors of 680 pF (TBD) in series. A charge leakage bleed-off resistor of ~10 megohms shall be incorporated on the low-voltage side of the capacitor pair. | A,D |
| 5.11.5 | PMT Bias Chain Load Resistor | A load resistor of ~10 kilohms shall be incorporated into the bias network. | A,D |

| Req | Title | Summary | Verif |
|---|---|---|---|
| 5.11.6 | PMT Bias Chain Dynode Decoupling | The resistors biasing the last three dynode stages shall be bypassed by capacitors to prevent excessive loading by very large pulses. | A,D |
| 5.12 | Radiation Tolerance | The ACD electronics shall remain within specifications after a total ionizing radiation dose of 10 kRad/Si. | A |
| 5.13.1 | ACD Electronics Reliability | No single failure in the ACD electronics shall result in complete loss of signal from more than one ACD PMT. The overall calculated reliability of an ACD event processor electronics board shall be at least 0.98 per year. | A |
| 5.13.2 | ACD System Reliability | The probability of the loss of both VETO signals from a specific scintillator tile shall be less than 1%/year (TBR). The probability of the loss of VETO signals from a scintillator ribbon shall be less than 5%/year (TBR). | A |
| 5.13.3 | Latchup Tolerance | The ACD electronics shall not be susceptible to latchup, or if susceptible, will autonomously detect a latchup aan recycle power on the affected part. | A |
| 5.13.4 | Single Event Upset Tolerance | A single event upset (SEU) shall not cause the ACD electronics to transition to an unsafe state. | A |
| 5.14.1 | Detector On/Off Commands | The ACD-TEM will implement commands to allow each group of 18 PMT's to be separately powered on and off. | A,T |
| 5.14.2 | Detector Gain Commands | The ACD shall implement adjustability of the high voltage applied to the group of 18 PMT's associated with a single board. | A,T |
| 5.14.3 | Electronics On/Off Commands | The ACD-TEM will implement commands to allow each ACD electronics board to be separately powered on and off. | A,D |
| 5.14.4 | VETO Threshold Commands | The ACD shall implement adjustability of the VETO threshold for each PMT | A,T |
| 5.14.5 | High-Threshold Commands | The ACD shall implement adjustability of the High-Threshold for each PMT | A,T |
| 5.14.6 | ACD Monitoring Commands | The ACD shall implement adjustability of the monitoring functions of the ACD electronics, including the Low-Threshold for each PMT | A,T |
| 5.14.7 | TACK Format | ACD compliance with ICD. | A,D |
| 5.14.8 | Command Format | ACD compliance with ICD. | A,D |
| 5.15 | Output Data Formats | ACD compliance with ICD. | A,D |
| 5.16 | Power Consumption | The ACD total electronics power consumption shall not exceed 37 W. | A,D |
| 5.17 | Total Electronics Mass | As defined in LAT-ACD Subsystem Mechanical Interface Control Document, LAT-DS-00241 | A,D |
| 5.18 | Environmental Requirements | The ACD electronics shall meet the structural and thermal environment requirements defined in the LAT-ACD Subsystem Mechanical Interface Control Document, LAT-DS-00241 | T,D,A |
| 5.19 | Performance Life | The ACD shall maintain the specified performance for a minimum of five years in orbit. | A |
| 5.20 | Operation in High Rate Conditions | The ACD photomultiplier bias supplies shall switch into a low-gain mode via ACD-TEM command to protect the phototubes in very high intensity particle conditions (> 10 kHz in an individual tile) such as the South Atlantic Anomaly. | A,T |
| 5.20.1 | Notification of Mode Change | The ACD shall identify times when it switches into low-gain mode for high counting rate conditions. | D,T |
| 5.20.2 | Tile Linear Response | Each ACD PMT and its associated electronics shall be capable of operating within the specifications above at MIP rates up to 3 kHz. | D,T |
| 5.21 | Testability | The ACD electronics shall incorporate additional capabilities as needed to enable thorough and efficient testing, throughout the GLAST mission, of the functions required of the ACD. | D |